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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,064	06/20/2003	Chad Allen Adams	ROC920030092US1	5653

7590 12/21/2004

Robert R. Williams
IBM Corporation - Dept. 917
3605 Highway 52 North
Rochester, MN 55901

EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,064	ADAMS ET AL.	
	Examiner	Art Unit	
	Son L. Mai	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,9,11,14 and 18-20* is/are rejected.

7)☒ Claim(s) *3-5,7,8,10,12,13 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06-20-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 6, 11, 19 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. As for claim 6, the limitations "said plurality of compare transistors" in lines 2-3 and "said common precharge node" in line 3 lack sufficient antecedent bases for these limitations in the claim.

4. As for claim 11, the recitation "deactivate driver circuit couples said enable redundant wordline signal to said two-high field effect transistor stack" is not accurate. Figure 2 and related text depicts the deactivate driver circuit (200) couples common precharge node signals (COMMON PRECHARGE), not the enable redundant wordline signal to the two-high, to the two-high field effect transistor stack.

5. As for claim 19, the claim cannot depend upon itself. Should it depend upon claim 18?

6. As for claim 20, the claim is rejected because in its dependency it includes the limitations of claim 19.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 2, 9, 14, and 18-20, as best understood in view of the above 112, second paragraph rejection, are rejected under 35 U.S.C. 102(b) as being anticipated by Koshikawa (U.S. Patent 6,272,057).

Regarding claim 1, Koshikawa discloses a redundancy circuit for a memory array comprising: a miscompare detector (22 in figure 1) for comparing a current address (XADD in figure 8) to be accessed with a memory defect address (in FUSE CIRCUIT 110 in figure 8), said miscompare detector providing an enable redundant wordline signal (REDUNDANCY DECISION SIGNAL) responsive to a match of the compared addresses (column 6, lines 46-64), a deactivate driver circuit (28, 30 in figure 1) coupled to said miscompare detector for disabling non-redundant wordlines responsive to said enable redundant wordline signal; and a redundant driver (N3 in figure 3) coupled to said miscompare detector for enabling redundant wordlines responsive to said enable redundant wordline signal.

Regarding claim 2, Koshikawa also teaches a wordline select circuit (34 in figure 8) coupled to said redundant driver (N3) for selecting a redundant wordline (80) responsive to said enable redundant wordline signal (REDUNDANCY DECISION SIGNAL).

Regarding claim 9, Koshikawa teaches the deactivate driver circuit (28, 30 in figure 1) generates a reset signal (PX3) to deactivate a non-redundant wordline decoder (32) responsive to said enable redundant wordline signal.

Regarding claim 14, Koshikawa teaches the redundant driver (N3 in figure 3) coupled to said miscompare detector (22) for enabling redundant wordlines (80) responsive to said enable redundant wordline signal includes a buffer circuit (N4, P6) receiving said enable redundant wordline signal (REDUNDANCY DECISION SIGNAL) and providing a buffered enable redundant wordline signal output.

Regarding claim 18, Koshikawa teaches a method (Abstract) for disabling non-redundant wordlines and for enabling redundant wordlines using a redundancy circuit for a memory array comprising the steps of: comparing a current address to be accessed with a memory defect address (column 6, lines 34-39), providing an enable redundant wordline signal (REDUNDANCY DECISION SIGNAL) responsive to a match of the compared addresses (column 6, lines 39-45), responsive to said enable redundant wordline signal, generating a reset signal (PX3) for disabling non-redundant wordlines (50 in figure 2), and responsive to said enable redundant wordline signal, activating a redundant wordline (80 in figure 3) for said memory defect address.

Regarding claim 19, Koshikawa also teaches the generated reset signal (PX3) deactivates a wordline decoder (32) for the memory array.

Regarding claim 20, Koshikawa teaches the method including the step responsive to a miscompare of the compared addresses, of allowing a normal access to a non-redundant wordline (column 7, lines 17-23).

Allowable Subject Matter

9. Claims 3-5, 7-8, 10, 12-13, 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 6 and 11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach at least the limitation of claim 10 which includes a deactivate driver circuit having a two-high field effect transistor stack coupled between a reset common node and ground. The prior art also fails to teach a miscompare detector including a plurality of compare field effect transistors coupled between a common precharge node and a common discharge node.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12-14-04

Son L. Mai
Primary Examiner
Art Unit 2818